ReMedPar
Medical Equipment Solutions

A Whitepaper from ReMedPar

Automated Test Equipment Methodologies For Diagnosis & Repair

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June 2009

Introduction

Automated Test Equipment (ATE) is a computer controlled device that is utilized to quickly test electronic components and assemblies. In the past, custom designed controllers or relay logic were used. An ATE system can be as simple as a Digital Multimeter (DMM) connected to a computer where data from the DMM is acquired, analyzed and stored. An ATE system can range from this simple example all the way to a large collection of sophisticated test equipment capable of diagnosing faults in complex electronic systems. The Flying Probe is an example of the most modern technology for rapid and sophisticated testing of electronic assemblies.

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Classically, ATE has been used to test a wide variety electronic devices after production. Today, the different types of ATE equipment available include Bed of Nails Testers, Automatic Optical Inspection (AOI), X-ray Inspection, In Circuit Test Equipment (ICT), JTAG Boundary Scan Testing, various varieties of computer interfaced test instruments and the Flying Probe. New versions of ATE are coming on the market each year.

ATE Has Improved and Expanded

In the past, the complexity and level of programmability, or lack thereof, relegated ATE only to high volume manufacturing environments. This was due to the nature of system configuration and fixture construction as well as the great amount of time to accomplish this task every time a new circuit was to be tested. With the development of computer technology and different methods of connectivity these shortcomings were reduced and the entire concept of ATE configuration has changed.

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Today, ATE is not just economically feasible in a high speed production environment. With the new programmability and connectivity options as well as expanded operating features of test equipment currently on the market, it makes sense to utilize ATE in a repair depot environment where it had not been previously practical. ATE reduces the diagnostic time required thus increasing productivity, throughput and quality of component level repair.

Over the past 20 years, many common pieces of test equipment have gained connectivity. These include Network Analyzers, Oscilloscopes, Function Generators, Power Supplies, Signal and RF Generators, Power Meters, Spectrum Analyzers and even DMMs. Connectivity methods available today include Serial (RS 232, RS 422 and Optically Isolated Serial), USB (Universal Serial Bus), Ethernet and GPIB (General Purpose Instrument Bus IEEE 488.2).

Additionally, other form factors of the aforementioned test equipment have come on the market. Various test instruments have been configured into a card format where several test equipment cards can be connected to a single backplane and share the same power supply with communication between them and the control computer effected over the common bus. The most popular bus configurations are VXI, PCI, LXI and VME. Normally, in this card rack configuration, a PC card is included which controls all of the test equipment cards which are capable of communicating with the PC card over the bus resulting in the fastest data exchange rate possible.

ATE Software

In order to set-up the test equipment, control the operation and acquire data, software is needed. Often, many manufactures make available simple data acquisition and logging software which is model specific. Additionally, more sophisticated ATE systems have their own operating systems and control software, again system specific. Software may also be custom developed for the application in such languages as C and Visual Basic.

There are other players on the ATE software market. National Instruments is one of them and has several different products one of which is LabVIEW. This software is capable of communication with the largest variety of modern test instruments and in quite a large number of communication modes. LabVIEW is capable of instrument set-up, control, data acquisition, data analysis and display. It is a graphical programming language which has virtual front panel and block diagram views. The functional blocks are drag and drop onto either view and then connected in the block diagram view by virtual wiring. Most of the programming is accomplished with the mouse and very little keyboard activity is required. LabVIEW has grown in capabilities over time and has become an invaluable tool for the ATE community as well.

Self-test capabilities vary greatly, and rarely, if ever, would pinpoint an individual or group of components like ATE would.

As many of the newest variety of electronic circuit assemblies employ embedded processors and controllers, many manufacturers have included self diagnostic software which performs a self test of blocks of circuitry. This self testing may be accomplished either at boot-up or on demand from the field service engineer. Between manufacturers, this capability varies greatly from go or no go testing to localization of circuit boards or individual circuits. It is rare, if ever, that a self test would pinpoint an individual or group of components like ATE would.

Now that a brief overview of ATE possibilities has been covered, let us take a bit more in depth look at some of the benefits and shortcomings of different ATE methodologies.

Bed of Nails ATE

A Bed of Nails Tester is a traditional electronic test fixture employing numerous pins held in an acrylic plate. An individual wire from each pin is then connected to a switching multiplexor, typically of the relay variety. Each of the spring loaded pins, referred to as “Pogo Pins” makes contact with various nodes on the printed circuit board of the DUT (Device Under Test). The DUT is pressed down against the hundreds or even thousands of pins allowing it to make contact with all of the nodes simultaneously. The DUT is held down on the bed of nails by either mechanical clamping action or vacuum.

It requires approximately 4 to 6 weeks to fabricate each of the bed of nails fixtures. This up-front time and costs associated with test fixture fabrication does not lend itself to the scenario where many different circuit boards must be tested.

Flying Probe

On the other end of the spectrum is the Flying Probe. A good example of a flying probe would be the Takaya APT-9411 CE. First and foremost, this style of tester is fixtureless and requires significantly less set-up time as it alleviates the necessity of creating a test fixture. Changes to the test to be run can be effected programmatically instead of having to re-work a fixture. This offers great flexibility in a high board mix where each board is low volume.

Takaya APT-9411 CE Flying Probe

The Flying Probe offers many different test modes such as resistance, capacitance, inductance, impedance, transistor test mode, Zener diode test mode, diode test mode, DC Voltage, AC Voltage, switching transistor/FET on testing, optocoupler on test and an IC Opens Test (in order to check for ESD damage to IC bond wires). The Flying Probe also has extra multiplexor ports which allow a myriad of other test equipment to be connected. JTAG software may be employed to boundary scan test BGAs (Ball Grid Arrays) and other CPLDs (Complex Programmable Logic Devices).

Running all of the above tests manually on a circuit board would be time prohibitive; however, with the Flying Probe, these tests can be accomplished in approximately 50 ms each or even faster in the combination test mode. This model also accommodates boards up to 25”x24”. Boards of this size may contain literally thousands of nodes which make it impractical to test with other methodologies.

This photograph depicts a DUT in the Takaya flying probe.

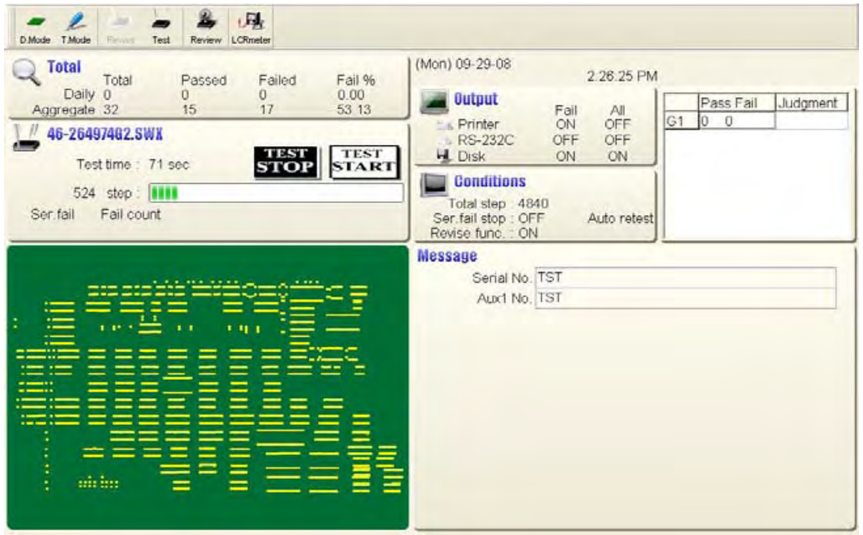
Notice the four probes in the center of the photograph and one of the two Machine Vision cameras (yellow and black object on the upper right hand side of the photo).

The Flying Proble is capable of a positioning resolution of 1.25 µM.

Many of the newer PCBs (Printed Circuit Boards) incorporate integrated circuits with extremely fine pitch lead spacing making it prohibitive to use a bed of nails tester or manually test without running the risk of bridging or shorting one or more of the package leads. The positioning ability of the Flying Probe offers the necessary precision to test even extremely fine pitched leads as it is capable of positioning resolution of 1.25 µM. It also has an X,Y positioning repeatability of 35 µM and requires a contact pad size of only 150 µM. The system has 4 separate probes and 3 axis positioners to minimize fly time and conduct the programmed tests efficiently.

The Flying Probe employs advanced image processing technology which ensures reliable and accurate automatic optical testing (AOT) with two Machine Vision Cameras. The AOT system also performs alignment functions on each of 3 fiducials allowing the program to position the probes exactly over the test points in cases of small clamping misalignment. The desired test points are located with the two cameras during the programming process greatly reducing programming time.

This screen shot shows a typical Takaya test mode display



Total

	Total	Passed	Failed	Fail %
Daily	0	0	0	0.00
Aggregate	32	15	17	53.13

46-26497402.SWX

Test time : 71 sec

524 step :

Ser.fail Fail count

(Mon) 09-29-08 2:26:25 PM

Output

	Fail	All
Printer	ON	OFF
RS-232C	OFF	OFF
Disk	ON	ON

	Pass Fail	Judgment
G1	0 0	

Conditions

Total step : 4840
Ser.fail stop : OFF
Revise func. : ON
Auto retest

Message

Serial No. TST
Aux1 No. TST

In this screen shot, the green area on the left shows the test point map on the DUT. Failure statistics of both boards and individual components are stored by the system. The message section on the right hand side of the screed displays individual component errors. Upon test completion, the Takaya Flying Probe will print a “Cash Register” style tape documenting the component, expected value and actual value of each failure. This methodology greatly reduces troubleshooting time of defective circuit boards.

Typical programming time for the Takaya Flying Probe is between 1 and 3 days depending on the DUT complexity. This time allows one to define the location of each node, assisted by the machine vision cameras. Once each node location is defined, a known good (golden sample) board is placed in the machine and the node values are learned. After a couple of passes on the golden sample, tolerances may be adjusted and the program is then complete.

JTAG Boundary Scan

Many of the circuit boards today contain BGAs of which most of the solder balls are inaccessible due to the fact that they reside underneath the chip. Additionally, many CPLDs are so complex that it makes it impractical to do type of evaluation other than a functional test. These problems are addressed by the IEEE 1149 standard. This standard was written by the Joint Test Action Group (JTAG) and the architecture is known as “JTAG boundary scan”. The standard is defined as a 5 pin serial protocol for accessing and controlling the signal-

The IEEE 1149 standard is defined as a 5 pin serial protocol for accessing and controlling the signal levels on the pins of a digital circuit.

levels on the pins of a digital circuit and has some extensions for testing the internal circuitry on the chip itself.

All the signals between the chip's core logic and its pins are intercepted by a serial scan path known as the "Boundary Scan Register". In normal operation, this register connects the core logic to the chip's pins. In the external test mode, it can disconnect core logic from the pins, drive the output pins by itself and read the latch states of the input pins. In the internal test mode, it can disconnect the core logic from the pins, drive the core logic input signals by itself and read the latch states of the core logic output signals. It does all this without disturbing what logic has been programmed into the core. Basically, JTAG boundary scan can exercise all input and output buffers as well as the tri-state buffers of a CPLD to indicate the health of the chip.

The JTAG interface uses the following signals that are available on every chip that supports the standard:

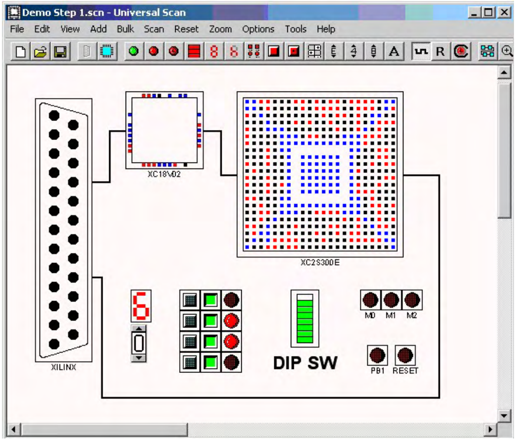
- TRST* (Test ReSeT) input which enables and disables the test interface.
- TCK (Test Clock) which controls the timing of the test interface independent of the chip.
- TMS (Test Mode Select) input which controls the state of the test interface.
- TDI (Test Data Input) which supplies data to the JTAG test registers.
- TDO (Test Data Output) which is the output of the JTAG test result data.

In addition to these signals, you would need a ground reference and a VDD voltage reference.

The TRST* signal is not always required when performing the boundary scan test. This leaves 4 signals (TCK, TMS, TDI and TDO) which fit nicely with the 4 probes on the Takaya Flying Probe. The ground and VDD voltage reference are available from two additional bottom probes which are available on the Flying Probe as well. Given this scenario, it is possible to add JTAG Boundary Scan Testing to the Flying Probe with but a little programming and wiring effort.

Most manufacturers chain the JTAG capable devices on a board during the design phase. All JTAG capable devices have TCD, TMS, TDI and TRST* signals paralleled so that these signals may be connected to only one device and all devices will receive these signals simultaneously. Also, the JTAG devices have inputs and outputs connected together in a daisy chain. Lacking a schematic, one can identify the JTAG signals from the chip manufacturer's data sheet, thus ignoring the chain and testing each chip one at a time.

This screen shot shows a JTAG user interface and the status of various pins of a CPLD and a BGA.



Just as with the Flying Probe, a known good board is scanned to determine the normal state of each chip's pins then the input and output pins are exercised and checked for chip functionality.

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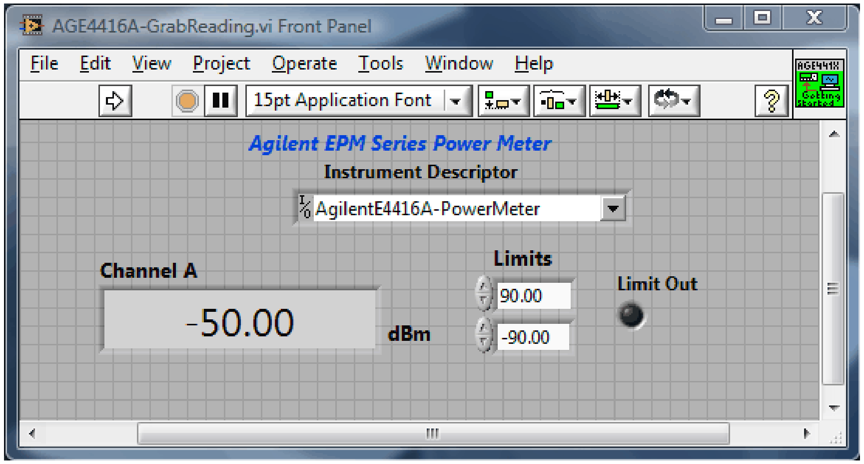
LabVIEW

LabVIEW is a graphical programming language for data acquisition and analysis. It is capable, with the right interface components, of communication over Ethernet, GPIB, USB, USB2, RS-232 and RS-422. A program in LabVIEW is referred to as a VI (Virtual Instrument) which is composed of Virtual Controls, Virtual Displays and other Vis which are considered to be sub Vis. Each program has two views being used during programming. The first is a Virtual Front Panel or GUI (Graphical User Interface) and the second is a Block Diagram View.

This illustration depicts a simple front panel for a VI which grabs readings from an Agilent E4416A Power Meter.



Agilent EPM Series Power Meter

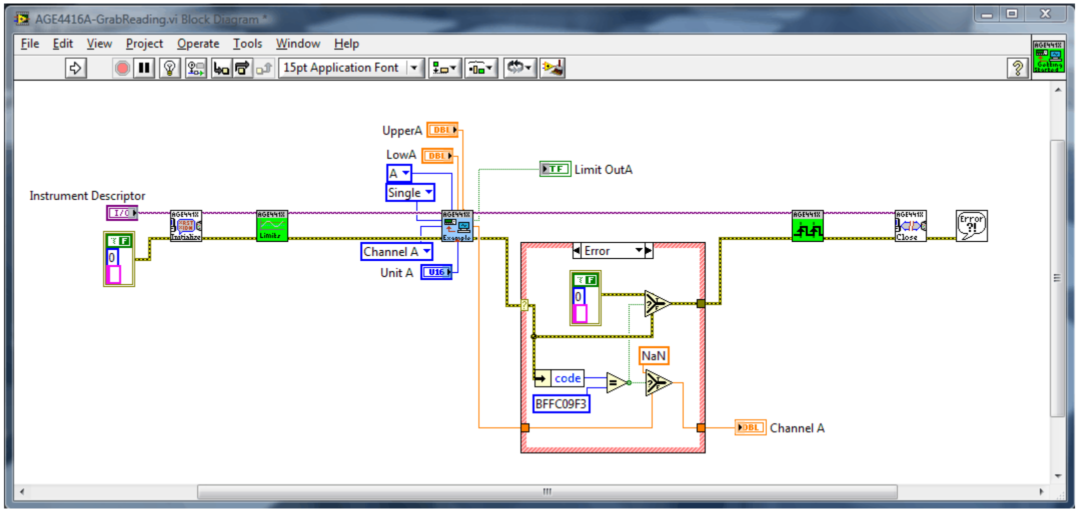
Instrument Descriptor: AgilentE4416A-PowerMeter

Channel A: -50.00 dBm

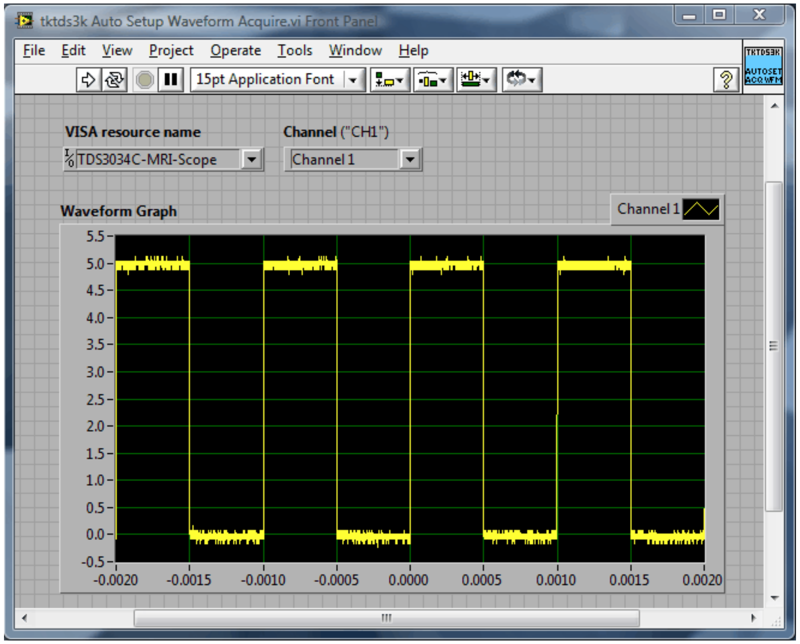
Limits: 90.00, -90.00

Limit Out: ●

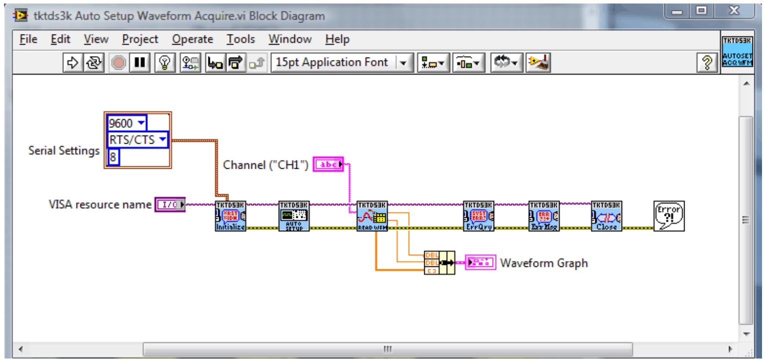
This illustration is the block diagram view of the same E4416A Power Meter VI.



Screen shot of a VI which grabs a trace from a Tektronix TDS3034C Oscilloscope.



This block diagram is quite simple due to the re-use of sub Vis.



LabVIEW also has many different data analysis tools. One could capture oscilloscope data as in the example above then analyze the data with analysis tools such as Spectral, Distortion, Tone, Dual Channel Spectral, Amplitude & Level, Timing & Transition, Curve Fitting, Filters, Statistics, Convolution & Correlation, Mask & Limit testing, Histogram and many other functions.

This data may be either saved as a spreadsheet file automatically by LabVIEW for later display in Microsoft Excel or passed to a report generation program such as DIAdem which is also written by National Instruments.

Diagnostic Data Analysis

Automated testing methods allow for repeatability. Set-up of whatever test instrument is being used will always be the same which serves to eliminate human error especially the more complex the set-up procedure is. Each time the test is run, the controlling software will perform a set-up routine on the associated test equipment which removes the human element from the equation allowing for precise and repeatable adjustment. Additionally, the automated process reduces the amount of time to set-up and adjust the test equipment from one assembly to another.

Data acquisition and transfer directly from the test instrument to the controlling computer increases accuracy of measurement readings.

Data acquisition and transfer directly from the test instrument to the controlling computer increases accuracy of measurement readings. Once again, we remove human interpretation from the equation and thus eliminate related human error in reading the data displayed on the test instrument. The automated data transfer greatly reduces the amount of time required to read and transcribe data for analysis.

The computer is also very good at data analysis and delivers extremely repeatable results however it does have its limitations depending on the analysis algorithms used. There are several common algorithms that can be utilized in order to determine good/bad, pass/fail or true/false status of the DUT. The three main algorithms are the high threshold, low threshold or delta methods.

High Threshold is a set point which determines if the acquired data point is <= the set point. Conversely, **Low Threshold** is a set point which determines if the acquired data point is >= the set point. With High and Low Threshold, everything is either black or white with no shades of grey in the decision process. These methods are absolute.

For example, we will work on a scale of 0 to 10 with a set point of 5 and a decision of pass/fail. Using the above parameters, if one sets a high threshold a reading of 4 results in a decision of pass determination while a reading of 6 results in a determination of fail. However, a reading of 5.1 results in a fail determination as would a reading of 5.001. With a low threshold, a reading of 6 results in a pass and a reading of 4 results in a fail. Also a reading of 4.999 results in a fail.

From this data, one can conclude that with a threshold algorithm, the reading would only result in a possible black/white determination. These algorithms do not allow for any shades of grey possibilities in their analysis. This is due to the basic fact that a computer only understands two numbers, 0 or 1, off or on, resulting in very finite results in a computer’s decision making capabilities.

The next method to discuss is the **Delta algorithm**. Delta means difference and functions like a tolerance and is often referred to as an “envelope” algorithm. We will use the preceding scenario of a scale of 0 to 10 with a set point of 5 but this time we will also use a delta value of 1. In a Pass/Fail decision if the reading is >6 or <4, a Fail determination will register while if the reading is >4 AND <6, a Pass determination will result. As you can see, the larger the delta value, the less precise the evaluation will be.

There are considerably more algorithms available for data analysis use but the preceding three are the most basic and the most often used. The final judgment is often open to interpretation however with automated testing many egregious failures are quickly sorted out.

With the bed of nails tester or the flying probe, the combined value of all components connected to the same node will influence the evaluation. Components are inspected one at a time however the value between two nodes is evaluated and any other components connected to either node may influence the outcome. This means that even though the component being tested may be good, it will register as bad if one of the other components connected to the two nodes being used to evaluate the desired component is defective. Bottom line is that more than one component may be evaluated as defective even though only one of them actually is. This is where the components marked as defective by the test system are open for interpretation as to if they are actually defective.

Conclusion

In conclusion, automated testing is just one more tool to speed the troubleshooting process and helps to pinpoint defective components which must be replaced. It is not a substitute for functional testing of an assembly in an entire system as proof positive that the assembly is capable of 100% functionality, but it greatly speeds up the process by weeding out many defective assemblies and locating failures before the functional test is attempted. ATE also adds yet another level of assurance that an assembly is fit for its intended use, and greatly increases repair and evaluation throughput and overall business productivity.

About ReMedPar

Founded in 1987, ReMedPar is the leading third-party medical parts provider for aftermarket diagnostic imaging and biomedical engineering equipment. For over 20 years ReMedPar has delivered on its mission to provide high quality and cost effective parts to keep critical equipment running. ReMedPar is unique in that we are not merely a part sourcing organization but a business with a long heritage in technical capabilities, extensive investment in quality assurance, and an expansive tested inventory line up. Our commitment to technical expertise is manifested in the many aspects of our business from parts identification, on time delivery of quality parts to in-depth technical training classes and unparalleled technical support. This results in quality parts that you can count on at the most cost effective price. For more information, visit **www.remedpar.com** or call us at **1-800-624-3994**.

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